PATENT APPLICATION
Attorney's Do. No. 5038-358

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of: Chuan Hu and Daoqiang Lu

Serial No. Not yet assigned

Filed: Concurrently herewith

For: FLUXLESS DIE-TO-HEAT SPREADER BONDING USING THERMAL INTERFACE MATERIAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Applicant submits herewith PTO Form 1449 listing patents and publications of which he is aware which may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR Section 1.56.

The above-referenced application is a divisional of U.S. Serial No. 10/436,677, filed May 12, 2003. It includes the same disclosure as U.S. patent application Serial No. 10/436,677.

It is understood that the listed references will be considered in the examination of the application and that no separate copies of the same prior art are required to be provided since they were previously cited or transmitted in the foregoing prior application. 37 CFR Section 1.98(d). Form(s) PTO 1449 is enclosed listing references cited by the Examining Attorney and submitted by applicant in the prior applications.

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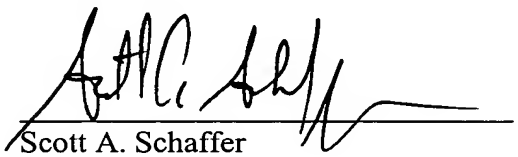
Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



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INFORMATION DISCLOSURE CITATION
FORM PTO-1449 (Modified)

U.S. PATENT DOCUMENTS

Exam Init	Ref	Document Number	Issue Date	Name	Class	Sub Class
_____	_____	6,471,115 B1	10/29/2002	Ijuin et al.		
_____	_____	6,495,397 B2	12/17/2002	Kubota et al.		

FOREIGN PATENT DOCUMENTS

Exam Init	Ref	Document Number	Publication Date	Country	Name
_____	_____				
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OTHER DOCUMENTS

Exam Init	Ref	Author, Title, Date, Pertinent Pages, Etc.)
		Klink et al., "Innovative Packaging Concepts for Ultra Thin Integrated Circuits," *IEEE 2001 Electronic Components and Technology Conference,* 5 pages (2001).
		Dodd et al., "Impact of Substrate Thickness on Single-Event Effects in Integrated Circuits," *IEEE Transactions on Nuclear Science,* Vol. 48, No. 6, p. 1865-1871 (December 2001).
		Sunohara et al., "Development of Wafer Thinning and Double-Sided Bumping Technologies for the Three-Dimensional Stacked LSI," *IEEE 2002 Electronic Components and Technology Conference,* p. 238-245 (2002).
		http://www.webelements.com/webelements/elements/text/Au/enth.html, *Mark Winter, The University of Sheffield,* 4 pages (3/6/2003).
		"Some Practical Suggestions for Solder Preform Design," *Indium Corporation of America,* 1 page (prior to 5/12/03).
		"Mechanical Enabling for the Intel® Pentium® 4 Processor in the 478-Pin Package," *Intel Corporation* (October 2001).

Examiner: _____

Date Considered: _____